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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/675,817	09/28/2000	Thomas Tomazin	10559-284001 / P9291- ADI	9781
20985 7590 11/19/2004 FISH & RICHARDSON, PC 12390 EL CAMINO REAL SAN DIEGO, CA 92130-2081			EXAMINER HARKNESS, CHARLES A	
			ART UNIT 2183	PAPER NUMBER

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/675,817

Applicant(s)

TOMAZIN ET AL.

Examiner

Charles A Harkness

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 September 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-8,18-21 and 23-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-8,18-21 and 23-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1, 3-6, 8, and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuraski, Jr. et al., U.S. Patent Number 6,260,134 (herein referred to as Zuraski) in view of Nishii et al, U.S. Patent Number 5,918,045 (herein referred to as Nishii) in further view of Narayan et al., U.S. Patent Number 6,161,172 (herein referred to as Narayan '172).

2. Referring to claims 1 and 21 Zuraski has taught a method of aligning instructions in a processor comprising:

storing a plurality of instructions of different sizes with the buffer area including a plurality of sub-buffers, each sub-buffer storing a unit instruction width with an instruction of greater than a unit instruction width stored in more than one sub-buffer (Zuraski Fig. 1B the unit instruction width is 8 bits, which includes instruction (a), but instruction (d) takes up two unit instruction widths)

aligning a first instruction from said buffer area (Zuraski abstract figure 2 reference number 18 column 6 lines 20-29);

decoding the size of the first instruction (Zuraski abstract figure 4 reference numbers 306,308,310, column 12 line 63-column 13 line 17);

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determining the beginning of a second instruction based on the size of the first instruction (Zuraski column 13 lines 18-22 figure 4 reference number 312);

decoding the size of the second instruction (Zuraski abstract figure 4 reference numbers 306,308,310, column 12 line 63-column 13 line 17; the same process would be repeated for other instructions).

3. Zuraski has not taught receiving data containing instructions in a plurality of sub-buffers, and receiving data containing instructions in a plurality of buffers, selecting at least one of said buffer areas to output said first instruction on an output part; and

determining whether processing the second instruction will deplete one of a plurality of buffer areas and instructing the plurality of buffer areas to receive additional instructions or

4. Nishii has taught determining whether processing the second instruction will deplete a buffers and instructing the buffer to receive additional data if processing the second instruction depletes the buffer (Nishii column 8 lines 38-60; since Nishii always keeps the prefetch buffer from being empty by comparing the two pointers and determining when the buffer needs to have more instructions fetched from memory, the system then knows when the next instruction, or number of instructions, will deplete the buffer). It would have been obvious to one of ordinary skill in the art at the time of the invention to determine when processing an instruction will deplete the instruction buffer and then to fetch more instructions. Prefetching increases the speed of execution by keeping the execution units busy and not stalled or waiting on instructions from memory, which operates at a slower pace (column 1 lines 5-10). Therefore, by fetching instruction ahead of time, before they are needed, the execution units, or pipeline, will not stall, thus decreasing the amount of time needed for execution. Therefore it would have been obvious

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to one of ordinary skill in the art at the time of the invention to use prefetching to decrease the amount of time needed for execution.

5. The combination of Zuraski and Nishii has not taught using a plurality of sub-buffers, and receiving data containing instructions in a plurality of subbuffers, selecting at least one of said plurality of sub-buffer areas to output said first instruction on an output part.

6. Narayan '172 has taught receiving data containing instructions in a plurality of buffers (Narayan '172 figure 4 reference numbers 86A-C; Narayan has taught using sub-queues), and selecting at least one of said buffer areas to output said first instruction on an output part (Narayan '172 figures 4 and 6, column 20 lines 18-33, column 23 lines 3-27). It would have been obvious to one of ordinary skill in the art at the time of the invention to have a parallel processing system, which would include buffers and storage in parallel. Having a plurality of buffers allows the system to execute in parallel, store the instruction in parallel, pass the instruction on to the alignment logic and to the decode in parallel (as shown in figures 4 and 6). By using parallel processing, more than one process, or task, is executed sequentially, meaning if two decoders are working in parallel, twice the instruction can be decoded at the same time. This, inherently, reduces the amount of time required for execution and speeds up the throughput of the system. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use parallel processing to increase the throughput of the system.

7. Referring to claim 22 the combination of Zuraski, Nishii, and Narayan '172 has taught further comprising storing the plurality of instructions in a plurality of sub buffers (Narayan '172 figure 4, the instructions are stored in the subqueues).

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8. Referring to claims 3 and 23 the combination of Zuraski, Nishii, and Narayan '172 has taught further comprising comparing a most significant bit of a pointer to a first sub-buffers to a most significant bit of a pointer to a second sub-buffers to determine whether processing one of the plurality of instructions will deplete a buffer (Nishii column 8 lines 38-60; Nishii shows enumerating the write and read pointer of the buffers to determine whether the buffer needs to have a request sent for more instructions).
9. Referring to claims 4 and 24 the combination of Zuraski, Nishii, and Narayan '172 has taught further comprising storing a first instruction across a plurality of sub-buffers prior to processing the instructions (Narayan '172 figure 4 the instructions are stored across the subqueues).
10. Referring to claim 5 the combination of Zuraski, Nishii, and Narayan '172 has taught further comprising adding the size of the first instruction to a current instruction position to determine the beginning of the second instruction (Zuraski column 13 lines 18-22 figure 4 reference number 312).
11. Referring to claim 6 the combination of Zuraski, Nishii, and Narayan '172 has taught further comprising aligning ahead a number of cycles equal to a cache latency (Nishii column 8 lines 38-60). Since Nishii has filled the prefetch buffer so that it will never be empty, the fetching is done equal to a cache latency, therefore allowing the alignment to occur at a cache latency since the alignment of Zuraski occurs after the instructions are fetched from memory.
12. Referring to claim 8 the combination of Zuraski, Nishii, and Narayan '172 has taught further comprising issuing a request to a memory to reload the plurality of buffers (Nishii column 8 lines 38-60).

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13. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Zuraski, Nishii, and Narayan '172 in view of Davis U.S. Patent Number 6,367,003 (herein referred to as Davis).

14. Referring to claim 7 the combination of Zuraski, Nishii, and Narayan '172 has not taught further comprising aligning instructions in a digital signal processor. Davis has taught further comprising providing the instructions in a digital signal processor (Davis column 1 lines 21-36). It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a system using a DSP (Digital Signal Processor). By using a DSP, the system is optimized for executing specific types of algorithms typically encountered in signal processing (Davis column 1 lines 23-26). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention would have implemented the system of Favor in a DSP setting to allow for optimized execution for types of algorithms which will increase the speed of execution.

17. Claims 18-20 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narayan '172 in view of Nishii.

18. Referring to claims 25 and 27 Narayan '172 has taught a processor comprising:

A plurality of buffer areas (Narayan '172 figure 4 reference numbers 86A-C), adapted to store a plurality of instructions of different width in a plurality of subparts, each of said subparts storing a unit instruction width, and said instructions of greater than unit instruction widths being stored in multiple said subparts (Narayan '172 column 6 lines 23-65);

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A multiplexor, connected to said plurality of subparts, and selecting and aligning one of said plurality of subparts from any of said subparts within said buffer areas as a current instruction (Narayan '172 figures 4 and 6, column 20 lines 18-33, column 23 lines 3-27).

20. Narayan '172 has not taught a predictor, operating to predict when at least one of the plurality of buffer areas will be empty, and to send a signal to instruct said at least one of the plurality of buffer areas to load another instruction data.

21. Nishii has taught a predictor, operating to predict when at least one of the plurality of buffer areas will be empty, and to send a signal to instruct said at least one of the plurality of buffer areas to load another instruction data (Nishii column 8 lines 38-60; since Nishii always keeps the prefetch buffer from being empty by comparing the two pointers and determining when the buffer needs to have more instructions fetched from memory, the system then knows when the next instruction, or number of instructions, will deplete the buffer). It would have been obvious to one of ordinary skill in the art at the time of the invention to predict when processing an instruction will deplete the instruction buffer and then to fetch more instructions. Prefetching increases the speed of execution by keeping the execution units busy and not stalled or waiting on instructions from memory, which operates at a slower pace (Nishii column 1 lines 5-10). Therefore, by fetching instruction ahead of time, before they are needed, the execution units, or pipeline, will not stall, thus decreasing the amount of time needed for execution. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use prefetching to decrease the amount of time needed for execution.

22. Referring to claim 26 the combination of Narayan and Nishii has taught wherein said predicting comprises comparing a most significant bit of a pointer to a first subportion, to a most

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significant bit of a pointer to a second subportion, to determine if any of the subportions will be depleted (Nishii column 8 lines 38-60; since Nishii always keeps the prefetch buffer from being empty by comparing the two pointers and determining when the buffer needs to have more instructions fetched from memory, the system then knows when the next instruction, or number of instructions, will deplete the buffer).

23. Referring to claim 18 the combination of Narayan '172 and Nishii has taught further comprising comparing a most significant bit of a pointer to a first subpart to a most significant bit of a pointer to a second subpart to determine whether processing one of the plurality of instructions will deplete any of the buffer areas (Nishii column 8 lines 38-60; Nishii shows enumerating the write and read pointer of the buffers to determine whether the buffer needs to have a request sent for more instructions).

24. Referring to claim 19 the combination of Narayan '172 and Nishii has taught further comprising aligning ahead a number of cycles equal to a cache latency (Nishii column 8 lines 38-60). Since Nishii has filled the prefetch buffer so that it will never be empty, the fetching is done equal to a cache latency, therefore allowing the alignment to occur at a cache latency since the alignment of Narayan '172 occurs after the instructions are fetched from memory.

25. Claim and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Narayan '172 and Nishii in view of Davis U.S. Patent Number 6,367,003 (herein referred to as Davis).

26. Referring to claim 20 the combination of Narayan '172 and Nishii has not taught further comprising aligning instructions in a digital signal processor. Davis has taught further comprising providing the instructions in a digital signal processor (Davis column 1 lines 21-36).

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It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a system using a DSP (Digital Signal Processor). By using a DSP, the system is optimized for executing specific types of algorithms typically encountered in signal processing (Davis column 1 lines 23-26). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention would have implemented the system of Favor in a DSP setting to allow for optimized execution for types of algorithms which will increase the speed of execution.

Response to Arguments

27. Applicant's arguments filed 09/03/04 have been fully considered but are moot based on the new grounds of rejection, and they are not persuasive.

28. In the response, Applicant argues that:

“Applicant contends that Narayan, alone or in combination with the other references, does not teach ‘a plurality of buffer areas, each buffer area including a plurality of sub-buffers.’”

29. This is not persuasive. Narayan '172 has taught using sub-queues to hold the instructions (figure 4 reference numbers 86A-C; Narayan has taught using sub-queues). Also, Applicant has claimed “a unit instruction width” and an instruction that is larger than a unit instruction width. Any of the prior art could be applied to this since a unit instruction width is not defined, and could simply be a bit, or several bits, in a queue or in the sub-queue in Narayan. Since there are instructions larger than the instruction width, as defined by Applicant, it is not necessary for the instruction width to be the same size as the instructions. Therefore, the sub-queues of Narayan would have sub buffers, or instruction width sized sections, inside of each sub-queue in which an instruction would overlap many of the sub buffers.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 571-272-4167.

The examiner can normally be reached on 9Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Allen Harkness

Examiner

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November 08, 2004



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